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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Fumitoshi MIZUTANI et al.
Title:	DATA PROCESSING APPARATUS AND DATA PROCESSING METHOD
Appl. No.:	10/827,433
Filing Date:	04/20/2004
Examiner:	Srinivasa R. Reddivalam
Art Unit:	2619
Confirmation Number:	2720

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of documents known to Applicants in order to comply with Applicants' duty of disclosure pursuant to 37 CFR §1.56.

A copy of each non-U.S. patent document and each non-patent document is being submitted to comply with the provisions of 37 CFR §1.97 and §1.98.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicants do not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97(c), before the mailing date of either a final action under 37 CFR §1.113, a notice of allowance under 37 CFR §1.311, or an action that otherwise closes prosecution in the application.

RELEVANCE OF EACH DOCUMENT

The documents listed on the attached PTO/SB/08 were cited as being relevant during the prosecution of the corresponding Japanese application. A partial English translation of the Japanese Office Action of November 25, 2008, follows:

> (Reasons) Reason 1
>
> The invention described in Claim 1 is a data processing device comprising multiple reception interfaces which receive the same data, wherein a reception interface unit performs communication error handling whereby data reception of different reception interface units is stopped and resending of data is requested from the data sender if an error occurs in the received data, while the invention described in Claim 6 relates to control in a data processing device comprising a transmission interface unit which transmits the transmitted data with the same timing to multiple data transmission destinations, wherein the transmission interface unit splits the transmitted data into data lengths which can be transmitted within a single predetermined clock signal to generate packet data, and each data packet is synchronized to a clock signal and transmitted with the same timing to multiple transmission destinations, which is not found to be a data processing device comprising multiple interface units which receive the same data wherein a reception interface unit performs communication error processing if an error occurs in the received data.
>
> Thus, the invention described in Claim 1 and the invention described in Claim 6 do not try to solve the same problem and differ in their substantial parts, and thus are not found to have the relationship stipulated in Article 37, Items 1 and 2 of the Patent Law.

In addition, these inventions are not found to satisfy any of the relationships stipulated in Article 37, Items 3, 4 and 5 of the Patent Law.

(Reasons) Reason 2

Claim 1 states "if an error occurs in the received data, data reception is stopped." Given the presence of an expression which contradicts the technical content that even though data is being received, the reception of data is stopped if an error occurs, the scope of the invention is not clear.

Thus, the inventions relating to Claims 1 through 5 are not clear.

(Reasons) Reason 3

(Claims) 1 through 5

(Cited Literature) 1 through 4

(Remarks)

Cited Literature 1 describes a processor having a first and second computation unit which operate in parallel to each other in duplex processor mode, wherein the processor comprises a third and fourth computation unit which continuously check for bit errors of data words read into the respective computation unit, and the processor uses the results of this check to determine which of the two computation units has outputted incorrect data if different output data has been outputted by the two computation units.

Cited Literature 2 describes a fault tolerant computer comprising a first processing unit, which is the main processing unit, and a second processing unit, which is an auxiliary processing unit, wherein each processing unit comprises a signal processing unit which executes data processing, an error detection unit which monitors if the signal processing unit is operating normally and detects errors, and a monitoring control unit which controls monitoring operations including detection of various errors, the received data from a communication line is received by both processing units and data processing is executed in parallel, and the two error detection units detect whether or not the signal processing units are operating normally, and if one of the monitoring control units detects

processing unit errors, the information is communicated to the other monitoring control unit.

Furthermore, notifying devices of the other system about detected errors in a duplex information processing device, and notifying the transmitting side to make it retry if an error is detected on the receiving side in data transfer processing between information processing devices is well known, as indicated in Cited Literature 3 through 4, and in data transfer processing between information processing devices, adding a sequence number to each packet and transmitting data in packet units is a common practice, so these are all matters which could be easily accomplished by a person skilled in the art.

Thus, it is found that the inventions relating to Claims 1 through 5 of the present application could have been easily invented by a person skilled in the art based on the inventions described in Cited Literature 1 through 4 and the well known art.

(Claim) 6

(Cited Literature) 5

(Remarks)

Cited Literature 5 describes a fault tolerant computer system comprising a duplex processing system, wherein each processing system comprises a CPU module, an I/O module, and a cross-link for performing communication between the CPU module and I/O module, and the two processing systems operate in lock step synchronization.

Thus, it is found that the invention relating to Claim 6 of the present application could have been easily invented by a person skilled in the art based on the invention described in Cited Literature 5.

If any reasons for rejection are newly discovered, a notification of reasons for rejection will be issued.

(List of Cited Literature)

1. Published Japanese Translation of a PCT Application 2001–526422

2. Japanese Unexamined Patent Application Publication 2001–290668

3. Japanese Unexamined Patent Application Publication H10–154085

4. Japanese Unexamined Patent Application Publication H02–264337

5. Japanese Unexamined Patent Application Publication H01–154242

Record of Prior Art Literature Search Results

- Fields searched IPC G06F11/16–11/20
  G06F15/16–15/177
  G06F11/14
  G05F13/00
  G05F15/00
  G06F11/28–11/34
  H04L1/00, 1/08–1/24
- Prior art literature Japanese Unexamined Patent Application Publication H11–296394
  Japanese Unexamined Patent Application Publication H04–071037

This record of prior art literature search results does not constitute a reason for rejection.

Document F1 is a U.S. counterpart of Document F2.

Any document listed on the attached PTO/SB/08 was cited as being relevant during the prosecution of the corresponding Japanese application. An English translation of the foreign-language documents has not been provided. The absence of a translation or an English-language counterpart document does not relieve the PTO from its duty to consider any submitted document (37 CFR §1.98 and MPEP §609). English language abstracts are attached.

Applicants respectfully request that each listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

STATEMENT

The undersigned hereby states in accordance with 37 CFR §1.97(e)(1) that each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three (3) months prior to filing of this Statement.

The undersigned hereby states in accordance with 37 CFR §1.704(d) that each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart application and that this communication was not received by any individual designated in 37 CFR §1.56(c) more than thirty days prior to the filing of the information disclosure statement.

Although Applicant believes that no fee is required for this Request, the Commissioner is hereby authorized to charge any additional fees which may be required for this Request to Deposit Account No. 19-0741.

Respectfully submitted,

Date: December 22, 2008

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